# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-311921

(43)Date of publication of application : 07.11.2000

(51)Int.Cl. H01L 21/60
H01L 21/56
H01L 23/12
H01L 23/29
H01L 23/31

(21)Application number : 11-120074

(22)Date of filing : 27.04.1999

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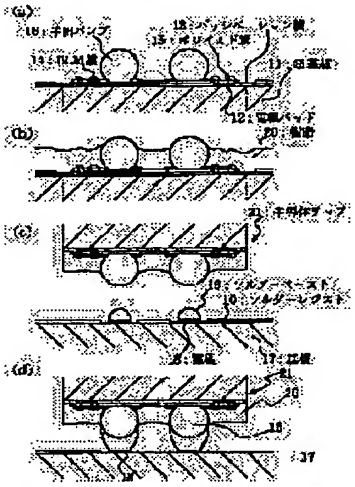
## (54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To obtain a semiconductor device and a manufacturing method thereof where a chip is bonded to a board via bumps and the reliability of the bump bonding is raised.

SOLUTION: For a semiconductor device manufacturing method comprising steps of forming metal (solder) bumps 16 in a wafer state, coating a resin 20 for protecting the wiring surface of a semiconductor chip 21 in a wafer state, and cutting the semiconductor chip 21 out of a wafer, the metal bumps 16 are bonded to the wiring surface of the chip 21 in the form of necked roots, and the resin 20 is coated to cover the roots of the metal bumps 16.



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[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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CLAIMS

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[Claim(s)]
[Claim 1] The semiconductor device characterized by having joined the metal bump to whom the bottom section was narrow on the substrate, having covered this metal bump's root headquarters, and carrying out coating of this substrate top face by resin.
[Claim 2] For said resin, Young's modulus is 2 about 1200 kgf(s)/mm. Semiconductor device according to claim 1 with which it is above, coefficient of linear expansion is about 20 ppm/degree C or less, and thickness is characterized by about 40-micrometer or more being about 110 micrometers or less.
[Claim 3] Said metal bump is a semiconductor device according to claim 1 with which it has the top face by which surface polish was carried out, and the difference of the height of this top face and the minimum coating thickness part of said resin is characterized by about 10-micrometer or more being about 50 micrometers or less.
[Claim 4] Said resin is a semiconductor device according to claim 1 characterized by inclining in the shape of skirt breadth in said metal bump's bottom section, and burying this bottom section.
[Claim 5] It is the manufacture approach of the semiconductor device which said metal bump is joined by the wiring side of a semiconductor chip in the configuration where of that bottom section is narrow, in the manufacture approach of a semiconductor device of having the process which forms a metal bump in the state of a wafer, the process which coat this resin that protects the wiring side of a semiconductor chip in the state of a wafer, and the process which separate said semiconductor chip from a wafer, and is characterized by for said resin to have covered said metal bump's bottom section, and for coating to be carried out.
[Claim 6] For said resin, coating is carried out by the spin coat method, and the Young's modulus of this resin is 2 about 1200 kgf(s)/mm. The manufacture approach of a semiconductor device according to claim 5 that it is above, coefficient of linear expansion is about 20 ppm/degree C or less, and thickness is characterized by about 40-micrometer or more being about 110 micrometers or less.
[Claim 7] The manufacture approach of a semiconductor device according to claim 5 that it has the process which grinds said metal bump's front face in the state of a wafer, and the difference of the height of this polished surface and the minimum coating thickness part of said resin is characterized by about 10-micrometer or more being about 50 micrometers or less.
[Claim 8] Said resin is the manufacture approach of the semiconductor device according to claim 5 characterized by carrying out coating so that it may incline in the shape of skirt breadth in said metal bump's bottom section and this bottom section may be buried.

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a semiconductor device and its manufacture approach. It is related with the amelioration for raising the reinforcement of a metal bump's joint in more detail.
[0002]
[Description of the Prior Art] CSP (Chip Size Package) etc. — the wiring side of IC chip faces a substrate directly with a semiconductor device, and it flows through the thing of a flip chip method with the circuit pattern of a substrate through the joint of the conductor by solder metallurgy, copper, or these alloys. However, since the coefficient of linear expansion to heat differs from the wiring substrate which generally consists of silicon and mainly consists of resin greatly, IC chip of a semi-conductor generates stress by the difference in an amount which expands with the heat received from a chip or a peripheral device at the time of a actual activity. In many cases, the weakest part from this stress is the joint of a package and a substrate, and, especially in the case of a flip chip method, there is no lead section, and since there are few parts which ease stress, it is necessary to raise the dependability of junction.
[0003] In the conventional flip chip method, in order to raise the dependability of junction, there was a method of aiming at improvement in junction dependability by joining and reinforcing the clearance between a substrate and a chip by the resin called under-filling. However, this approach worsens reworkability of a package. Therefore, the junction between a substrate and a chip was joined only with solder, and the reliable approach of junction was desired.
[0004] In order for wafer level to perform resin spreading for wafer surface protections on a spin coat on the manufacture approach also in a flip chip method in the structure (refer to below-mentioned drawing 4 (f)) like EBC (Encapsulated Bump Chip) by which packaging is carried out, the coating thickness of coating resin is influenced by the Young's modulus of resin, and viscosity.
[0005] In order for resin to give the property that it can apply in uniform height in predetermined time when giving and carrying out the spin coat of the function which raises a bump's junction dependability to this resin although what is necessary is just to use the resin of the low viscosity in low Young's modulus if the material property of resin has selectivity innumerably and resin is only used as a wiring protective coat, it is necessary to select the resin to be used proper.
[0006] Moreover, since the coating thickness of resin influences greatly the operation of a bump's plane of composition which reinforces especially a plane of composition with IC chip for the below-mentioned reason, setting out of proper coating thickness is needed.
[0007]
[Problem(s) to be Solved by the Invention] Drawing 6 (a) shows the junction condition of the solder bump of a semiconductor package (EBC), and a substrate. A semiconductor chip 2 is carried on a substrate 1. A semiconductor chip 2 is joined on a substrate 1 through the primary bump 3 of solder, and the secondary bump 4 of solder.
[0008] If a temperature reduction happens to this semiconductor package (semiconductor device), as shown in A and B, respectively, a shrinkage force will act on a substrate 1 and a semiconductor chip 2. In this case, the amount of contraction of A of a substrate 1 becomes larger than the amount of contraction of B of a semiconductor chip 2 by the difference in coefficient of linear expansion. Therefore, as shown in drawing 6 (b), according to this expansion difference (difference of the amount of

contraction), a package deforms, and as shown in this drawing (c), tensile stress C occurs in a solder bump's joint.

[0009] The part where a solder bump breaks in response to stress is three between a primary bump and a secondary bump between a chip, between solder and a substrate, and solder as possibility. However, in a bump's formation, if the plane-of-composition product is equivalent respectively, the part which may break first will usually become between a chip and solder. Since a substrate side has the low Young's modulus of the substrate itself, this reason is for absorbing distortion directly under a soldered joint side, and is because there is no relaxation device which absorbs such distortion in IC chip plane-of-composition side. Moreover, although the layer will become weak if Cu of solder and a joint is exposed to an elevated temperature and makes an alloy layer, the frequency exposed to heat is also because there are more planes of composition with IC on the process of manufacture.

[0010] That is, in the structure like a flip chip method, when making junction to a substrate hold by soldered joint, and each plane-of-composition product between IC chip, between solder and a substrate, and solder is almost the same, in order to raise the life of solder, it is important to raise the bonding strength between IC chip and solder.

[0011] The stress generating condition between this IC chip and solder is shown in drawing 6 (b) and (c) as mentioned above. For example, suppose that the substrate with which IC chip was mounted was cooled from 100 degrees C to 0 degree C. Deformation of the substrate at that time will be in the condition of curving like drawing 6 (b) since the amount of contraction of a substrate is large compared with IC chip. The stress which mainly acts on the solder in this case is tensile stress as shown in drawing 6 (c).

[0012] A crack tends to go into the bottom part of a soldered joint, and this part becomes easy to break by such tensile stress. Especially the bottom part of solder is narrow and, in the case of the bump of a configuration thinner than a center section, the effect of such thermal stress becomes large.

[0013] This invention aims at offer of the semiconductor device which raised the dependability of bump junction, and its manufacture approach in consideration of the above-mentioned conventional technique in the semiconductor device which joins a chip through a bump to a substrate.

[0014]

[Means for Solving the Problem] In order to attain said object, in this invention, the metal bump to whom the bottom section was narrow on the substrate is joined, and the semiconductor device characterized by having covered this metal bump's root headquarters and carrying out coating of this substrate top face by resin is offered.

[0015] Since the bottom part of the metal bump to whom the bottom section of bump junction became thin is covered and reinforced by resin according to this configuration, the dependability of junction improves.

[0016] By this invention, if the principle of this reinforcement operation is explained further, as shown in drawing 1 (a), a substrate 1 and a semiconductor chip 2 are joined by the metal bumps 5, such as solder which consists of a primary bump 3 and a secondary bump 4, and the circuit forming face (underside side of drawing) of a semiconductor chip 2 is covered by the resin 6 for protection. The bottom part of junction of this metal bump 5 is covered with resin 6, and is embedded.

[0017] In such a configuration, at the time of a temperature reduction, as mentioned above, thermal stress occurs, tensile stress C acts on the plane of composition P between the metal bump 5 and a semiconductor chip 2, and this tensile stress C acts in the direction which exfoliates junction of the metal bump's 5 bottom section. This is coped with, and with this invention structure, at the time of cooling, the resin 6 by which coating was carried out to the semiconductor chip 2 generates a shrinkage force D, as shown in drawing 1 (a). This shrinkage force D acts in the direction which cancels the exfoliation operation by tensile stress C. By this, the metal bump's 5 bottom part is reinforced, the bonding strength of a plane of composition P increases, junction dependability improves, a junction life is prolonged, and the function stabilized over the long period of time is attained.

[0018] For said resin, at the desirable example of a configuration, Young's modulus is 2 about 1200 kgf(s)/mm. It is above, and coefficient of linear expansion is about 20 ppm/degree C or less, and thickness is characterized by about 40-micrometer or more being about 110 micrometers or less.
[0019] According to this configuration, it is the Young's modulus of resin about 1200 kgf(s)/mm 2 By considering as the above, the practically proper effectiveness of the reduction in stress by resin is acquired. In this case, although not limited especially about an upper limit, what is necessary is just the range of the Young's modulus obtained with the usual resin ingredient. Similarly, about coefficient of linear expansion, by carrying out [ degree C ] in about 20 ppm /or less, the practically proper effectiveness of the reduction in stress is acquired, and the practically proper low stress effectiveness is acquired by being referred to as about 40-110 micrometers about the thickness of resin (refer to below-mentioned drawing 2 ).
[0020] Drawing 2 shows the effectiveness of the reduction in stress by two kinds of resin. For Resin A, Young's modulus is 2 720 kgf(s)/mm. Coefficient of linear expansion is 34 ppm/degree C, and, for Resin B, Young's modulus is 2 1430 kgf(s)/mm. Coefficient of linear expansion is 17 ppm/degree C. It turns out that effectiveness is larger than the one where the one where Young's modulus is higher is lower. In this case, in order to apply resin to 40 micrometers or more by thickness uniform on a wafer for example, in a spin coat, resin with Young's modulus high to some extent must be used. Therefore, by enlarging thickness of this resin, resin with high Young's modulus will be used and the synergistic effect is acquired.
[0021] In the still more desirable example of a configuration, said metal bump has the top face by which surface polish was carried out, and the difference of the height of this top face and the minimum coating thickness part of said resin is characterized by about 10-micrometer or more being about 50 micrometers or less.
[0022] According to this configuration, when the difference of the height on a bump top face and the top face of resin sets to about 10 micrometers - 50 micrometers, the shrinkage force of proper resin with sufficient balance acts to the plane of composition of the tip side, and the plane of composition by the side of a substrate, and a proper low stress operation is acquired. If it is less than 10 micrometers, and the exfoliation force from resin is too strong and a difference becomes large from 50 micrometers to the plane of composition by the side of a substrate, an operation of the reduction in stress to the plane of composition of the tip side will become small too much.
[0023] If this is explained further, when spreading height (thickness) H of resin 6 is made the same as the primary bump's 3 height h in drawing 1 (a), since the shrinkage force D of resin 6 turns into tensile stress, it will enlarge the exfoliation force over a plane of composition Q on the contrary as an operation seen from the plane of composition Q.
[0024] Therefore, when it enlarges not much, the exfoliation force is made to increase to a plane of composition Q, although it is better to enlarge thickness of resin 6 if possible if it sees from a plane of composition P.
[0025] Relation between the stress concerning the soldered joint section and the thickness of resin is graph-ized by above-mentioned drawing 2 . This graph shows the alternating stress width by the temperature cycle of the solder section at the time of setting a primary bump's height to 110 micrometers. Since the stress of a plane of composition Q will become high if the stress of a plane of composition P is high and the thickness of resin becomes large when there is little thickness of resin, it turns out that the thickness of resin has a proper value (extremal value) to the stress of solder.
[0026] Although the value of this extremal value is changed a little according to the class of a chip size and substrate etc., when the height of primary Bengbu is set to h, it has a proper value (extremal value) with extent lower 10-50 micrometers than h in general. In addition, although the thickness of resin poses a problem with what height since it will become the configuration which rises like drawing 1 (b) and covers a bump's 7 side face with surface tension around a bump, if the spin coat of the resin is carried out in this case, the thickness of the resin said here says the thickness in the part which is not

influenced by these surface tension.
[0027] In the still more desirable example of a configuration, said resin is characterized by inclining in the shape of skirt breadth in said metal bump's bottom section, and burying this bottom section.
[0028] According to this configuration, for a wrap reason, the reinforcement of reinforcement increases [ resin ] a bump's bottom part in the shape of skirt breadth in the useless configuration which is not, and the dependability of junction improves further.
[0029] The process which forms a metal bump in the state of a wafer as the manufacture approach of the semiconductor device further applied to above-mentioned this invention in this invention, In the manufacture approach of a semiconductor device of having the process which coats this resin that protects the wiring side of a semiconductor chip in the state of a wafer, and the process which separates said semiconductor chip from a wafer Said metal bump is joined by the wiring side of a semiconductor chip in the configuration where the bottom section was narrow, and the manufacture approach of the semiconductor device characterized by for said resin having covered said metal bump's bottom section, and coating being carried out is offered. Thereby, the semiconductor device of above-mentioned this invention can be manufactured suitably.
[0030] In such a manufacture approach, coating of said resin is preferably carried out by the spin coat method, and the Young's modulus of this resin is 2 about 1200 kgf(s)/mm as mentioned above. It is above, coefficient of linear expansion is about 20 ppm/degree C or less, and thickness is about 40 micrometers or more about 110 micrometers or less.
[0031] It has still more preferably the process which grinds said metal bump's front face in the state of a wafer, and the difference of the height of this polished surface and the minimum coating thickness part of said resin is about 10 micrometers or more about 50 micrometers or less as mentioned above.
[0032] In this manufacture approach, still more preferably, coating of said resin is carried out so that it may incline in the shape of skirt breadth in said metal bump's bottom section and this bottom section may be buried as mentioned above.
[0033]
[Embodiment of the Invention] The gestalt of operation of this invention is explained with reference to a drawing below. Drawing 3 (a) – (d) is the important section sectional view showing the manufacture process of the semiconductor device concerning the gestalt of operation of this invention in order.
[0034] As shown in drawing 3 (a), the electrode pad 12 of aluminum (aluminum) is formed on the Si substrate 11 of a wafer condition, and the passivation film 13 which consists of Si3N4 and polyimide film is formed. BLM which connected with the electrode pad 12 and was rearranged on this Si substrate top 11 (Ball Limiting Metal) The film 14 is formed. Moreover, in order to give bump ****** for protection of the maximum front face, the polyimide film 15 is formed. The solder bump 16 is joined on the BLM film 14.
[0035] Next, as shown in this drawing (b), coating of the resin 20 is carried out by the spin coat on the Si substrate 11 of this wafer condition. As resin 20, the resin of an epoxy resin system, for example, 1.6-screw (2.3 epoxy POROKISHI) naphthalene, is used. This is equivalent to the resin A of above-mentioned drawing 2 , and the height relation between the thickness of coating or a bump is as above-mentioned.
[0036] Next, the semiconductor chip 21 of the above-mentioned configuration is cut down from a wafer at a dicing process, and a substrate 17 is made to counter, as shown in this drawing (c). An electrode 18 is formed on a substrate 17 and the solder paste 19 is formed on it. A substrate top face is covered by the solder resist 10.
[0037] Then, as shown in this drawing (d), a semiconductor chip 21 is joined by the flip chip method to a substrate 17, and the electrode 18 of a substrate 17 and the solder bump 16 of the tip side are connected.
[0038] Drawing 4 (a) – (d) and drawing 5 (e) – (g) is the explanatory view showing the process of the semiconductor device manufacture approach concerning the gestalt of operation of this invention in

order in more detail. In this operation gestalt, as first shown in drawing 4 (a), two or more semiconductor chips 21 are formed on the Si substrate 11 of a wafer 22. The configuration of this semiconductor chip 21 is the same as what was explained by above-mentioned drawing 3 .

[0039] Next, as shown in drawing 4 (b), resin 20 is coated with the condition of a wafer 22 with a spin coat on the Si substrate 11. The cure of this resin 20 is carried out at about 120-150 degrees C, and the fixed consolidation of each solder bump 16 is carried out including a bottom part.

[0040] Next, as shown in this drawing (c), the resin which ground the solder bump's 16 upper part and has covered this upper part is removed. This polish is ground to homogeneity to a bump's overall diameter (part which has swollen most). Thereby, it considers as the refresh side where solder exposed each solder bump top face. Thereby, primary bump 16a is formed.

[0041] Next, as shown in this drawing (d), printing spreading of the cream solder 25 is carried out on primary bump 16a by cream solder print processes using a squeegee 24 through a mask 23.

[0042] As this cream solder 25 is hardened in the condition of having rounded off for example, by wet back heat treatment and is shown in drawing 5 (e), secondary bump 25a is formed on primary bump 16a, bump height is made high and the highly reliable bump 26 is formed.

[0043] Then, the dicing of this semiconductor chip 21 is carried out, and it starts from a wafer (this drawing (f)), and joins on a substrate 17 like above-mentioned drawing 3 (c) and (d) ( drawing 5 (g)).

[0044] In addition, it is [ relaxation / of the stress concentration which prepares the difference of elevation between the top face of the resin 20 by which the spin coat was carried out, and the refresh side of ground primary bump 16a, and this generates in the plane of composition of primary bump 16a and secondary bump 15a ] good in drawing.

[0045] As mentioned above, while the resin on the top face of a bump is removed by a primary bump's polish, the effectiveness which extends the area of the plane of composition itself is also acquired by it. When the plane of composition of this primary bump and a secondary bump is narrow like above-mentioned drawing 1 (a) and thin, it is desirable to coat so that it may cover by resin also to this plane of composition, and to aim at reinforcement of sufficient bump. In addition, a bump is not limited to solder but can form with metals, such as Au and an alloy of Cu or others.

[0046]

[Effect of the Invention] Since the bottom part of the metal bump to whom the bottom section of bump junction became thin is covered and reinforced by resin in this invention as explained above, the dependability of junction improves. Thereby, the stress of a bump part declines and the dependability over the temperature cycle of a semiconductor package improves.

[0047] Moreover, although the flip chip mold semiconductor package was difficult to enlarge since the stress concerning a solder bump would increase if it enlarges, the large-sized semiconductor package which carried the big circuit becomes realizable by reinforcement of the resin of this invention. Moreover, since it is not necessary to reinforce the soldered joint section with under-filling material, reworkability improves. Moreover, it becomes unnecessary to prepare the bump for reinforcement, many the parts and bumps for wiring can be prepared, and high density wiring is attained, using a tooth space effectively.

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2.**** shows the word which can not be translated.
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## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The basic configuration explanatory view of this invention.
[Drawing 2] The graph which shows the effectiveness of this invention.
[Drawing 3] The process procedure explanatory view of the semiconductor device manufacture approach of this invention.
[Drawing 4] The explanatory view of another semiconductor device manufacture process procedure of this invention.
[Drawing 5] The explanatory view of the process following the procedure of drawing 4 .
[Drawing 6] The explanatory view of the trouble of the conventional semiconductor device.
[Description of Notations]
A substrate, 2:semiconductor chip, a 3:primary bump, a 4:secondary bump, 5 : 1: A metal bump, 6 : Resin, 7:bump, a 11:Si substrate, 12:electrode pad, 13:passivation film, 14: The BLM film, 15:polyimide film, 16:solder bump, a 16a:primary bump, 17:substrate, 18:electrode, 19:solder paste, 20:resin, 21:semiconductor chip, 22:wafer, 25:cream solder, a 25a:secondary bump, 26: Bump.

[Translation done.]